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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/070,035 | 07/03/2002 | Gilbert Wolrich | 10559-306US1 | 9914 |

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| EXAMINER | |
|---|---|
| PAN, DANIEL H | |
| **ART UNIT** | **PAPER NUMBER** |
| 2183 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 12/22/2006 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/070,035 | WOLRICH ET AL. | |
| | Examiner | Art Unit | |
| | Daniel Pan | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,5 and 7-22* is/are pending in the application.

4a) Of the above claim(s) *4 and 6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 7-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-3, 5, 7-22 are presented for examination. Claims 4,6 have been canceled.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1,10,16, 19 are rejected under 35 U.S.C. 101 because The reasons are given below.

3. As to claims 1,19, claims 1, 19 are not limited to tangible embodiment. in view of Applicant's disclosure, specification page 2, lines 6-13, the computer program product is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., (microprocessor )) and intangible embodiment ( e.g. (internet). Although applicant amended the program product residing on a computer readable medium for causing the execution, no practical application can be found in the clamed invention. The examiner understands the program product being stored in the computer readable medium to cause execution , but the focus is not on whether the steps taken to achieve a particular result is useful, tangible, concrete, but rather the final result is useful, tangible and concrete (see newly updated MPEP 2106, 2100-10-12 ). Claim 1 recites to cause execution, and it is read as a step taken to achieve practical result, but it is not a final result. Claim 1 also recites to branch to an instruction at a specific address at a value of availability of resource, but no

substantial practical application can be found in the claim. As such, the claim is not useful, tangible and concrete, and is therefore non-statutory.

4. As to applicant's remark that claims 1 and 19 achieve a final result determination of how program flow of the currently executing instruction sequence of instruction stream is to proceed, the determination of how the program would go is an intended result, not a positive limitation.

5. As to claim 10, no substantial practical application can be found in the claim. The practical application of the performance of the branch is not clear.

6. As to claim 16, although claim additionally recites the register stack and arithmetic unit coupled to the register stack, it is read as general arrangement of the system components, and present no substantial practical application. The practical application of the performance of the branch operation cannot be found.

7. As to the newly amended each of the microengine having control logic and execution box including the arithmetic logic unit and general purpose register set, and configured to process plurality of threads, since applicant taught in his specification (see page 2, lines 1-13) that his processor is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., (microprocessor )) and intangible embodiment ( e.g. freeware operating system available over the internet), it raised a doubt as whether applicant is seeking non-statutory subject matter. Furthermore, the practical application of plurality of threads is not clear. Moreover, the "control logic" is an abstract idea.

8. Although applicant recites the computer program product residing in a computer readable storage medium, it is neither a computer component nor statutory process, as it is not "act" being performed. The claimed computer program product does not define any structural and functional interrelationships between the computer program product and other claimed elements of a computer which permit the computer program product's functionality to be realized. In fact the computer's elements are being clearly defined. And, no substantial practical application can be found for the execution of instruction stream and the plurality of the threads.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claim 1 rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 29 (claim 29 includes limitations of parent

claim 23) of U.S. Patent No. 6,668,317. Although the conflicting claims are not identical, they are not patentably distinct from each other because although patented claim 29 did not recite the branch to the instruction at a specific address as claimed, patented claim 29 did disclose the determination of witch thread to execute based on signal indicating the completion of requested (see patented claim 23, lines 10-14). It would have been recognizable to one of ordinary skill in the art that the determination of the thread could be a sequence of instructions with the leading instruction at a specific memory location or a predefined address. Although not specifically recited, one of ordinary skill in the art should be able to recognize the applicability of branching or pointing to the instruction at the specified address as claimed based on the execution of the thread determination.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1,19 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Cage (4,454,595) in view of Kiefer (6,223,208) .

11. As to claims 1, 19, Cage taught a system including at least :

a) causing an executing instruction stream (see the sequence of code in fig.5a) to branch to an instruction at an a specified address (address not explicitly shown, but see the branch to the SER REQUEST command ) if a state or an evaluated state (Y/N 528), of a specified state name (BUFFER AVAIL), the state indicating the availability of a resource (available) of the data processing is a specified value [Y] (see how the program sequence branched to 526 in col.14, lines 1-23, see also the program sequence in fig.5 was contained in program code which was stored in a PROM in col.13, lines 1-6).

12. Cage did not explicitly show his instruction (see the SER REQUEST command) was at a specified address a clamed. However, Cage in the same patent taught the program sequence in fig.5 was contained in program code which was stored in a PROM in col.13, lines 1-6). Therefore, the commands including the SER SERIVCE command in the program code must be resided in a specific location in the PROM. And, it must included a specified address as claimed.

13. Cage did not specifically show the microengine having a control logic and execution logic including the arithmetic unit and general purpose unit , and configured to process a plurality of threads as claimed. However, Kiefer taught the microengine (see fig.2 [200] ) having a control logic [context switching] and execution logic including the arithmetic unit [260]-[250] and general purpose unit [register set] , and configured to process a plurality of threads (see the general purpose register and the execution of threads in col.8, lines 4-45). It would have been obvious to one of ordinary skill in the art to use Kiefer in Cage for including the microengine having a control logic and

execution logic including the arithmetic unit and general purpose unit , and configured to process a plurality of threads as claimed because the use of Kiefer could provide Cage the capability to process a plurality of threads according to the corresponding arithmetic units, and it could achieved by predefining the arithmetic unit and the plurality of threads into the configuration file of Cage with modified system parameters, such as the thread type, and read. write ports of arithmetic unit, and because Cage also taught an execution of a loop by a disk controller in an idle state and returned the loop after the command status form the floppy disk controller ((see col.5,lines 23-65), which was a suggestion of the need for including a thread, a task, or the like, in order to adapt to specific processing of the device, in doing so , provided a motivation.

14. Claims 1,10,19, rejected under 35 U.S.C. 103(a) as being unpatentable over Aggarwal et al. (6,275,508) in view of Kiefer (6,223,208).

15. As to claim 1, Aggarwal taught a system including at least :
a) causing an executing instruction stream to branch (see the branch instruction in fig.12) to an instruction at an address specified in the instruction (branch address) if a state , of a specified state name , indicating a resource availability value (see the condition of microengine in col.4, lines 64-67, col.5, lines 1-9) of a specified state name address field) was a specified value (see branch address in col.10, lines 12-31).
16. Aggarwal did not specifically show the microengine having a control logic and execution logic including the arithmetic unit and general purpose unit , and configured

to process a plurality of threads as claimed. However, Kiefer taught the microengine (see fig.2 [200] ) having a control logic [context switching] and execution logic including the arithmetic unit [260]-[250] and general purpose unit [register set] , and configured to process a plurality of threads (see the general purpose register and the execution of threads in col.8, lines 4-45). See reasons of obviousness in paragraph below.

17. As to claims 10, 19, Aggarwal taught :

a) evaluating a value of a specified state name (see the selector of the conditional branch in col.10, lines 20-31 ), the state name indicating available resource (see microengine in 4, lines 64-67, col.5, lines 15-)2), and performing a branching operation based on the value of the specified state name being set or cleared (see also the microengine decision on 0 or 1 bit in col.6, lines 56-65).

18. Aggarwal did not specifically show the microengine having a control logic and execution logic including the arithmetic unit and general purpose unit , and configured to process a plurality of threads as claimed. However, Kiefer taught the microengine (see fig.2 [200] ) having a control logic [context switching] and execution logic including the arithmetic unit [260]-[250] and general purpose unit [register set] , and configured to process a plurality of threads (see the general purpose register and the execution of threads in col.8, lines 4-45). It would have been obvious to one of ordinary skill in the art to use Kiefer in Aggarwal for including the microengine having a control logic and execution logic including the arithmetic unit and general purpose unit , and configured to process a plurality of threads as claimed because the use of Kiefer could provide Aggarwal the ability to accept a plurality of threads according to the corresponding

arithmetic units, and it could achieved by predefining control parameters of the arithmetic unit and the plurality of threads into the configuration file of Aggarwal so that specific control and arithmetic units and the threads Kiefer could be recognized by Aggarwal, and because Aggarwal also taught a sequencer for conditional branch to a next instruction (see col.10, lines 14-31), which was an indication of the applicability of a specific task, such as a process or thread , into Aggarwal to enhance the processing efficiency of the system, from the above, provided a motivation.

19. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa (5,724,563) in view of Kiefer (6,223,208).

20. As to claims 1 , Hasegawa disclosed a decisions on the direction of the instruction processing based on the state or condition (see also fig-s, and fig.10, see also the implicit value Z or C encoded in opcode in Table 1 , col.1 , lines 41-52, see the specific structure of also the teaching of Z and C flags set and reset in col.11, lines 14-40, lines 54-67, col.12, lines 1-5).

21. Hasegawa taught a data processing system including a branch instruction that caused an execution of instruction stream to branch to an instruction at an address (x) specified in the instruction if a state, of a specified name (Z,C), indicating the availability of a resource (see the branch instruction format in fig.2, see the value specified in the branch instruction field , see also fig.5, and fig.10, see also the implicit value Z or C encoded in opcode in Table 1 , col.11, lines 41-52, see also the teaching of Z and C flags set and reset in col.11 , lines 14-40, lines 54-67, col.12, lines 1-5). the parallel processor , see the pipeline processor in fig.6).

22. Hasegawa did not specifically show the process of a plurality of threads as claimed. However, Kiefer taught the microengine (see fig.2 [200] ) having a control logic [context switching] and execution logic including the arithmetic unit [260]-[250] and general purpose unit [register set] , and configured to process a plurality of threads (see the general purpose register and the execution of threads in col.8, lines 4-45). It would have been obvious to one of ordinary skill in the art to use Kiefer in Hasegawa for including the plurality of threads as claimed because the use of Kiefer could increase the processing bandwidth of Hasegawa, and it could be done by predefining the plurality of threads into Hasegawa with modified configuration variables (e.g. thread length and thread type), and because Hasegawa taught a pipeline processing for processing a plurality of instructions in parallel by dividing the execution process into a plurality of processing stages (see col.1, lines 10-17), which was recognizable by one of ordinary skill in the art to use threads, or processing stages, as claimed in order to increase the processing bandwidth (e.g. the parallel processing ), and in doing so, provided a motivation.

23. As to claims 2,3, see the arithmetic flags set or reset in col.11 , lines 19-32).

24. As to the parallel processor , see pipeline processor in fig.6.

25. As to claim 4, Hasegawa also included micro engines (see fig.9 instruction register 8, instruction decoder 3 and execution unit 11).

26. As to claim 6, see Branch 3, N in fig.5, see also the encoded branch opcode in Table 1 , for example, the first entry is (Branch on not equal Z). "Branch" being "br inp state" "Z " being the state name, and the X being the label, the number 3 was an optional token.

27. As to claim 5, Hasegawa also specified the number of instructions top execute before performing the branch (see 5g.5 Branch 3, X, see also fig.10).
As to claims 8,9 Hasegaga also included performing the branch based on specified name (see branch on over flow set and branch on overflow clear in Table I, see the flags set and reset in col.11, lines 14-35, see also the encoded flags in col.1, lines 42-52). As to the parallel processor , see the pipeline processor in col.5, lines 30-31).

28. As to claims 10,11, 12, 19,20, Hasewaga also evaluated a value of a specified state name, and the value of the state name indicating the available resource (Z flag) and performing a branching operation based on the value (Z=0/1) of the specified state name being set or cleared (see Branch 3, N in fig.5, see also the encoded branch opcode in Table 1 , for example, the first entry is (Branch on not equal Z). "Branch" being "br inp state" . "Z", being the state name, and the X being the label, the number 3 was an optional token.

29. As to claim 13, Hasegawa also included a label IxJ as a target filed (see the target address (x) in fig.5).

30. As to claims 14,15, Hasegawa also included an optional field for executing number of instructions before performing the branch (see fig.2 (23), see fig.5 Branch 3 X, see also fig.I6, see col.5, lines 55-67, see col.6, lines 24-32). As to the programmer, Hasegawa instruction was also programmable (see the application program set token in col.1, lines 42-44).

31. As to claims 16, Hasegawa also included a register stack (see fig.1 (register file) and a arithmetic unit (not explicitly shown as ALU, but it showed arithmetic calculations in col.1, lines 20-25, col.7, lines 44-52, see the adder in col.7, lines 52-56, fig.1 , see counter section 4 in col.7, lines 8-26 for the increment and decrement, and comparison of the counter, see also the calculation section 7 in col.63-67, col.8, lines 1- 4, and see also the arithmetic result flags in col.11 , lines 25-32). See also the branch on' over flow set and branch on overflow clear in Table 1 for the feature of evaluating the specified value.

32. As to claim 17, Hasegawa did not explicitly show the additional microengine as claimed. However, Hasegawa , in the same patent, taught the parallel processor pipeline processor 200) could be implemented in two kinds of hardware having respective different instructions set for use the same program code for both hardware (see col.13, lines 7-12). Therefore, additional hardware (or microengine ) was applicable in Hasegawa.

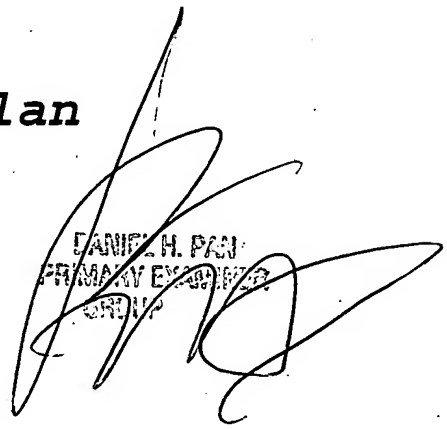
33. As to claim 18, Hasegawa also included target field (x) (see fig.5).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

***21 Century Strategic Plan***



Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :02/26/02,12/03/04,12/06/04,06/04/04, 11/16/05.